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Insightful Analysis of Processor Technology

ADESTO TARGETS IOT USING CBRAM

“Moneta” Nonvolatile Memory Reduces Power

By David Kanter (February 22, 2016)

Adesto’s conductive-bridge RAM (CBRAM) is a novel nonvolatile memory that’s CMOS compatible. The new Moneta device, the company’s second-generation CBRAM product, is designed to replace discrete EEPROMs in embedded and IoT applications. It can be used for both code storage and data logging. Relative to EEPROMs, Moneta has 50–100x better power for data accesses and 5x better idle power as well as easier system integration. It also boasts unique radiation tolerance.

Compared with flash memory, CBRAM uses a fundamentally different data-storage mechanism that relies on changing the cell resistance through an electrochemical process. It employs lower, CMOS-compatible voltages for programming and can be formed in a logic process with just a few extra steps. NAND and NOR flash, by comparison, are difficult to integrate with CMOS and require special process technology. To establish a solid record for the technology in the embedded market, Adesto offers Moneta as a discrete component, placing a special emphasis on applications that benefit from low power (e.g., IoT) and high radiation or thermal tolerances (e.g., medical).

Adesto Starts with Real Silicon

Adesto is one of the few recent Silicon Valley startups that actually designed silicon. CEO Narbeh Derhacobian, VP of Engineering Shane Hollmer, and VP of Marketing Ishai Naveh founded the company in 2007. All have extensive experience in the memory-chip industry, including stints at AMD (Spansion), Emosyn, Silicon Storage, Tower Semiconductor, and Virage. Michael Kozicki, a professor at Arizona State University, developed the concept of CBRAM in 1996. The technology was then licensed to Adesto, Infineon, Micron, and others. Adesto was the first company

to master the manufacturing process and successfully commercialize the technology.

The company raised \$48 million in several venture-funding rounds. To accelerate and protect its CBRAM technology, it acquired related patents and intellectual property from the failed memory company Qimonda (formerly Infineon) in 2009. Adesto’s first CBRAM product, dubbed Mavriq, entered production in 2011; millions of units have already shipped. Altis, a specialty foundry, builds the CBRAM chips in its Corbeil-Essonnes (France) fab.

In 2012, Adesto expanded its chip lineup by acquiring Atmel’s flash-memory business in another fire sale. It currently offers two flash families: the Fusion serial NOR chips, which typically store boot code, and the DataFlash E-Series, which provides byte-wide access for data logging. UMC fabricates these products.

Last fall, Adesto launched a public offering that valued the company at nearly \$90 million. It reported 2015 revenue of \$43 million, up 4% from the previous year, but it suffered a small net loss. The standard flash products continue to provide the bulk of the company’s revenue as well as a base of hundreds of customers that could switch to CBRAM over time. Adesto expects its revenue to rise more than 30% in 2016 as shipments of its new CBRAM products grow.

Flash Programming Is Hard

Flash memory is the de facto standard for nonvolatile memory. Thanks to the introduction of 3D NAND, the industry has simultaneously avoided lithography challenges and improved the physics that determine bit-cell endurance (see [MCR 11/17/14](#), “NAND Goes Vertical for Density”). Although 3D NAND enables continued density scaling, it’s even less amenable to CMOS integration than

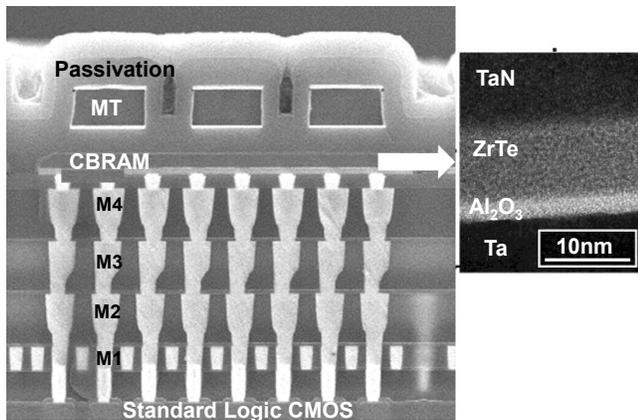


Figure 1. CBRAM bit-cell operation. Programming a CBRAM forms the eponymous conductive bridge across the metal-oxide dielectric. An erase operation does the reverse. (Source: Adesto)

is planar NAND because the extra layers would add cost and complexity to a CMOS chip. The technology still relies on charge-trapping or floating-gate bit cells, which use the same program/erase (P/E) mechanism for writing data.

Programming a NAND or NOR cell requires applying a high voltage (e.g., 5V) to the control gates of the target bit cells, causing electrons to move up through the cell (e.g., a floating gate) via tunneling. The electrons are trapped in the floating gate, thus making NAND flash memory nonvolatile. Erasing works in reverse by applying a high voltage to the channel and releasing electrons from the bit cell.

The program/erase mechanisms for NAND flash create two problems for CMOS integration. First, CMOS natively supports operation below 1V owing to the silicon bandgap. Generating the high voltages for P/E cycles requires charge pumps, which consume large area and require special high-voltage transistors that add to process cost. These transistors are also needed throughout the NAND flash macros (e.g., for row and column decoders). Second, the NAND P/E cycles consume a lot of energy. For

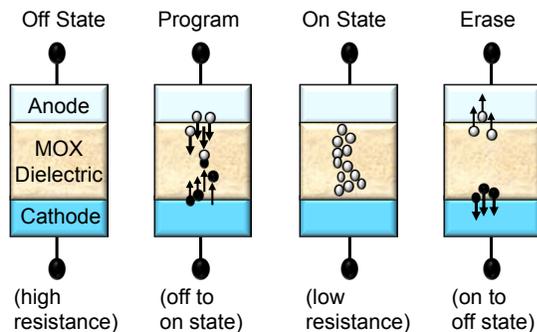


Figure 2. CBRAM bit cell. This structure is formed in the interconnect stack after the transistors and several metal layers. It comprises a bottom cathode, an insulator, and a top anode. (Source: Adesto)

systems with small batteries, such as wearable devices and some remote IoT sensors, writing to NAND flash can quickly drain the battery.

A Conductive Bridge to CMOS

Adesto's conductive-bridge RAM uses a new bit cell that solves both of these problems, enabling full integration of logic and nonvolatile memory. The CBRAM bit cell comprises an access transistor in series with a programmable conductive bridge. The bridge resistance depends on the voltage applied through the access transistor during programming.

Figure 1 shows a physical and logical view of the CBRAM bit cell, which is formed above several metal layers; a layer of tantalum is the cathode, sputtered amorphous Al_2O_3 is an insulator, and sputtered amorphous zirconium telluride is the anode. A conductive bridge of tellurium atoms forms across the insulator between the anode and cathode. Creating the conductive-bridge bit cell requires two extra mask steps, although one of the masks is fairly loose in pitch.

Figure 2 illustrates the various states and operations of the CBRAM bit cell. In the off state, the Al_2O_3 insulator is intact and creates high resistance. The programming operation works by applying 2.5V through the access transistor to the ZrTe anode, which causes tellurium atoms to move into the insulator, creating a low-resistance conductive bridge.

The erase operation works in reverse by applying an opposite voltage through the access transistor to the anode, which causes the tellurium to return to the anode, restoring the high-resistance path in the memory cell. In theory, varying the resistance of the bridge could enable multi-level cells, although this has not been demonstrated. Similar to NOR flash, the minimum program/erase granularity is a single byte. A read operation applies approximately 1V to the access transistor to determine whether the bit cell is in the high- or low-resistance state.

In a paper delivered at the 2013 Symposium on VLSI Circuits, Adesto presented a CBRAM bit cell that achieved read energy of 1pJ per bit and program energy of 50pJ per bit. Compared with NAND flash, CBRAM's read energy is roughly 10x lower and its program energy is an impressive 100x lower. The latency of read and write operations is generally similar to that of NAND flash.

Since the CBRAM cell physically changes during programming, it has some very attractive properties. First, unlike most nonvolatile memories, it can retain data across a very wide temperatures range. Second, the data is largely immune to radiation (e.g., x-rays and gamma rays), unlike in DRAM.

Show Me the Moneta

Adesto positions its new Moneta family as an alternative to EEPROM for basic data storage in systems with a micro-

controller (MCU). The CBRAM-based chip uses a standard SPI interface and is fabricated in an older 130nm process to yield modest 32–256Kb capacities (4–32KB).

Although the Moneta products are discrete components, the CMOS fabrication plays a significant role in reducing system cost and power consumption. As Table 1 shows, Moneta requires two or three input voltages: a core supply of roughly 1V, an I/O supply of 1.65–2.75V (which the company selected on the basis of customer preference), and a write supply. Although writes use 2.5V internally, Adesto specifies the write supply at 3.6–4.4V to provide sufficient margin. The core supply can use the same regulator as the attached microcontroller, reducing cost relative to standard EEPROMs. Read-only applications can omit the third input voltage.

As Table 1 indicates, Moneta's power consumption is dramatically lower compared with a standard EEPROM. In fact, it's so low that a small capacitor can provide sufficient energy to write 32 bytes of data into the CBRAM. Adesto claims that reading 500Kb/s of data consumes a paltry 10 microwatts—equivalent to 10pJ per bit, which is roughly 120x more efficient than a standard EEPROM. When writing 10Kb/s, Moneta consumes 7.5 microwatts, or 0.75nJ per bit—about 50x less than a standard EEPROM. The memory is rated for 10,000 write cycles (which is similar to flash) with an endurance of 10 years. Each Moneta memory includes a 128-byte one-time-programmable security register: 64 bytes contain a unique ID and 64 bytes are available to the user.

Moneta runs at a fairly slow 1MHz and is fed by a single serial bus. But the internal read and write latency for the CBRAM cells is much faster, roughly equivalent to NAND flash memory. As a result, the chip can enter a very low power state between transactions, consuming only 50 nanowatts.

When used for data storage, the Moneta architecture also improves overall system-level efficiency. The CBRAM includes a 32-byte write buffer, which enables the microcontroller to write out data and immediately shut down or go to sleep without waiting for an acknowledgement.

Moneta's Market Focus

Moneta targets embedded applications where CBRAM's low power and other unique characteristics are particularly valuable. These applications include traditional embedded markets (e.g., Bluetooth LE devices) as well as emerging markets (e.g., IoT beacons and sensors). A 256Kb memory sells for \$0.45 in 10,000-unit quantities—a modest premium relative to traditional EEPROMs.

A 256Kb Moneta device logging 128 bytes per minute will consume only 1.6mAh over four years, a fraction of the capacity of even a small button cell. For conventional systems, this low power consumption means incrementally smaller batteries and lower bill-of-materials (BOM) cost. More interestingly, it's ideal for energy-harvesting devices,

Price and Availability

Adesto offers Moneta in configurations ranging from 32Kb to 256Kb. The 256Kb version sells for \$0.45 in 10,000-unit volumes and is scheduled for production in 1Q16. For details, access www.adeptotech.com.

which generate power from the environment (e.g., thermal, solar, or vibration) rather than from a discrete battery.

Moneta's more robust data-storage technology is better suited to medical devices than traditional memories are. Some medical applications require sterilization, which often involves radiation (e.g., electron beams or gamma rays). These treatments can cause flash memory to lose data, whereas CBRAM will still retain data and function correctly.

Eventually, industrial, military, and aerospace applications may become more-profitable (albeit lower-volume) niches that can take advantage of CBRAM. Selling into these markets, however, is complicated and may be best left to a partner that licenses the technology.

Crossing the Commercialization Bridge

CBRAM is a novel technology that offers unique advantages to the semiconductor industry, but it remains at a relatively early deployment stage. One of its biggest selling points is compatibility with a CMOS logic process. Moneta reduces system power and cost by sharing a voltage regulator with the host microcontroller and potentially consolidating data logging and EEPROM functions into a single discrete component. Target applications include medical devices, which can take advantage of the radiation tolerance, as well as IoT beacons and logging, which benefit from CBRAM's low power consumption.

Although Adesto has shipped CBRAM products (e.g., Mavriq) in modest volumes, the technology has not been used for full on-die integration. A microcontroller with CBRAM integrated on die would be impressive and require far lower system power and cost than a system with a discrete component. To accomplish this integration, Adesto

Parameter	Adesto Moneta	Standard EEPROM
Core Supply Voltage	0.97–1.03V	Not Applicable
I/O Supply Voltage	1.65–2.75V	Not Applicable
Single Supply Voltage	Not Applicable	1.7–5.5V
Read Power (500Kb/s)	10µW	1250µW
Lowest Power-Down Mode	.05µW	.25µW
Clock Frequency (Max)	1MHz	20MHz
Operating Temp Range	–40 to +85°C	–40 to +85°C
Write Supply Voltage	3.6–4.4V	1.7–5.5V
Write Power (10Kb/s)	7.5µW	375µW

Table 1. Moneta versus standard EEPROM. The Moneta family is available in 32–256Kbit capacities. Although it requires more voltage inputs than standard EEPROM, the power savings are substantial. (Source: Adesto)

would have to adapt its CBRAM for a leading logic foundry rather than the tiny Altis fab. Leading microcontroller vendors may be wary of using CBRAM for high-revenue products until Adesto has established a stronger history with discrete components.

Adesto faces the normal set of challenges for any new technology, and it's following the old adage of "crawl, walk, run." After crawling with Mavriq, the company has proven

that CBRAM is robust and reliable, and it has established a toehold in the market. Taking advantage of this experience, the second-generation Moneta delivers reductions in cost and power that allow it to walk into new markets. Customer response has been strong, with design wins nearly doubling over the previous year. After rolling out Moneta, Adesto will be ready to accelerate and increase the integration level. ♦

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