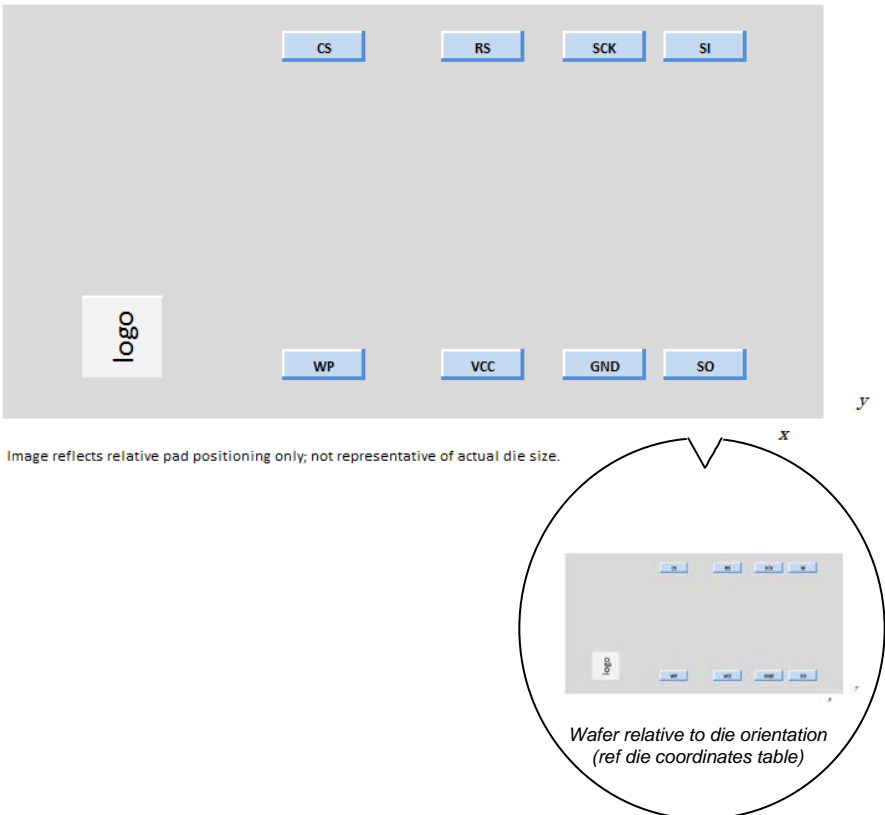


WAFER PRODUCT DATASHEET (ADDENDUM)

Product	AT45DB021E-DWF																																								
Description	2Mbit, DataFlash, 1.65V – 3.6V VCC																																								
Die Map	 <p>Image reflects relative pad positioning only; not representative of actual die size.</p> <p>Wafer relative to die orientation (ref die coordinates table)</p>																																								
Die Size & Pad Coordinates	<table border="1"> <thead> <tr> <th></th> <th>X (μm)</th> <th>Y (μm)</th> </tr> </thead> <tbody> <tr> <td>Die Size</td> <td>1844</td> <td>1360</td> </tr> <tr> <td>Scribe Line Width</td> <td>80</td> <td>80</td> </tr> <tr> <td>Die Step</td> <td>1924</td> <td>1440</td> </tr> <tr> <td>Pad Opening</td> <td>65</td> <td>65</td> </tr> <tr> <td>SI</td> <td>766.63</td> <td>592.35</td> </tr> <tr> <td>SCK</td> <td>534.57</td> <td>592.35</td> </tr> <tr> <td>RSB</td> <td>303.84</td> <td>592.35</td> </tr> <tr> <td>CSB</td> <td>75.04</td> <td>592.35</td> </tr> <tr> <td>WPB</td> <td>93.27</td> <td>-596.85</td> </tr> <tr> <td>VCC</td> <td>344.16</td> <td>-596.85</td> </tr> <tr> <td>GND</td> <td>655.15</td> <td>-596.85</td> </tr> <tr> <td>SO</td> <td>812.41</td> <td>-596.85</td> </tr> </tbody> </table>			X (μm)	Y (μm)	Die Size	1844	1360	Scribe Line Width	80	80	Die Step	1924	1440	Pad Opening	65	65	SI	766.63	592.35	SCK	534.57	592.35	RSB	303.84	592.35	CSB	75.04	592.35	WPB	93.27	-596.85	VCC	344.16	-596.85	GND	655.15	-596.85	SO	812.41	-596.85
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Technical Details	
Adesto Product Family	DataFlash
Density	2 Mbit
Operating Vcc	1.65V - 3.6V
ESD	>2kV JESD22-A114
Delivery Option	Wafer- unsawn
Wafer Size (mm)	200
Process Geometry (nm)	110
Die ID	637F4
Wafer Map	Electronic- text file
Manufacturing Facility	UMC
Wafer Thickness (µm) Maximum	725
Back Grind Options	None / Contact Adesto
Back Plane Connection	Floating / Not Required
Backside preparation / metallization	None
Bond wire qualified	AU <input checked="" type="checkbox"/> CU <input type="checkbox"/> AG <input type="checkbox"/>
Passivation Material	HDP oxide + SiON
Passivation Thickness (Å)	21000
Bond Pad Material	Ti/TiN/AlCu
Bond Pad Thickness (Å)	6000
Good Die per Wafer	Contact Adesto ¹
Active Circuits underneath the bond pad	Yes

¹ Average value; subject to change without notice.

Part Number Ordering Code ²	Operating Temperature Range	Functional Specification
AT45DB021E-DWF	-40°C to 85°C	http://www.adestotech.com/wp-content/uploads/doc8789.pdf

² Handle product in accordance with UV and ESD precautions.

Adesto Technologies Corporation

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Revision Level – Release Date	History
A – August 2015	Initial release.
B – November 2015	Updated wafer orientation in die map image. Added footnote on handling.
C – August 2017	Updated address and contact information.

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