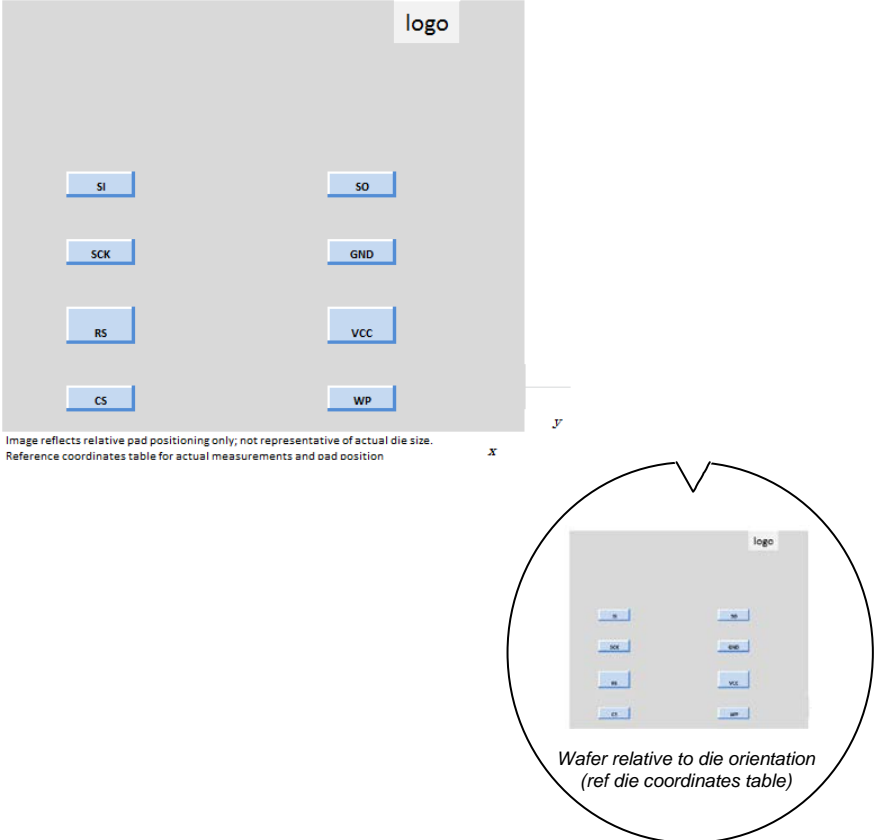


WAFER PRODUCT DATASHEET (ADDENDUM)

Product	AT45DB081E-DWF																																								
Description	8 Mbit, DataFlash, 1.7V – 3.6V VCC																																								
Die Map	 <p>Image reflects relative pad positioning only; not representative of actual die size. Reference coordinates table for actual measurements and pad position</p> <p>Wafer relative to die orientation (ref die coordinates table)</p>																																								
Die Size & Pad Coordinates	<table border="1"> <thead> <tr> <th></th> <th>X (μm)</th> <th>Y (μm)</th> </tr> </thead> <tbody> <tr> <td>Die Size</td> <td>1570</td> <td>2282</td> </tr> <tr> <td>Scribe Line Width</td> <td>80</td> <td>80</td> </tr> <tr> <td>Die Step</td> <td>1650</td> <td>2362</td> </tr> <tr> <td>Pad Opening</td> <td>65</td> <td>65</td> </tr> <tr> <td>SI</td> <td>-711</td> <td>-261.26</td> </tr> <tr> <td>SCK</td> <td>-711</td> <td>-501.26</td> </tr> <tr> <td>RSB</td> <td>-711</td> <td>-741.26</td> </tr> <tr> <td>CSB</td> <td>-711</td> <td>-1021.26</td> </tr> <tr> <td>WPB</td> <td>711</td> <td>-971.69</td> </tr> <tr> <td>VCC</td> <td>711</td> <td>-691.69</td> </tr> <tr> <td>GND</td> <td>711</td> <td>-451.69</td> </tr> <tr> <td>SO</td> <td>711</td> <td>-211.69</td> </tr> </tbody> </table>			X (μm)	Y (μm)	Die Size	1570	2282	Scribe Line Width	80	80	Die Step	1650	2362	Pad Opening	65	65	SI	-711	-261.26	SCK	-711	-501.26	RSB	-711	-741.26	CSB	-711	-1021.26	WPB	711	-971.69	VCC	711	-691.69	GND	711	-451.69	SO	711	-211.69
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Technical Details	
Adesto Product Family	DataFlash
Density	8 Mbit
Operating Vcc	1.7V - 3.6V
ESD	>2kV JESD22-A114
Delivery Option	Wafer- unsawn
Wafer Size (mm)	200
Process Geometry (nm)	110
Die ID	637F6
Wafer Map	Electronic- text file
Manufacturing Facility	UMC
Wafer Thickness (µm) Maximum	725
Back Grind Options	None / Contact Adesto
Back Plane Connection	Floating / Not Required
Backside preparation / metallization	None
Bond wire qualified	AU <input checked="" type="checkbox"/> CU <input type="checkbox"/> AG <input type="checkbox"/>
Passivation Material	HDP oxide + SiON
Passivation Thickness (Å)	21000
Bond Pad Material	Ti/TiN/AlCu
Bond Pad Thickness (Å)	6000
Good Die per Wafer	Contact Adesto ¹
Active Circuits underneath the bond pad	Yes

¹ Average value; subject to change without notice.

Part Number Ordering Code ²	Operating Temperature Range	Functional Specification
AT45DB081E-DWF	-40°C to 85°C	http://www.adestotech.com/wp-content/uploads/DS-45DB081E_028.pdf

² Handle product in accordance with UV and ESD precautions.

Adesto Technologies Corporation

3600 Peterson Way, Santa Clara, CA 95054 | phone: (408) 400-0578 fax: (408) 400-0721 | www.adestotech.com

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Revision Level – Release Date	History
A – August 2015	Initial release.
B – November 2015	Updated wafer orientation in die map image. Added footnote on handling.
C – August 2017	Updated address and contact information.

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