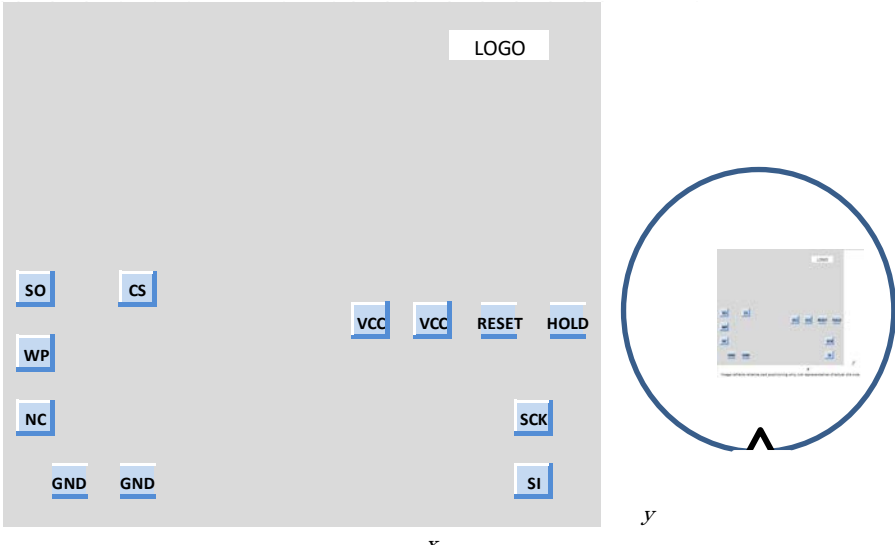


**WAFER PRODUCT DATASHEET (ADDENDUM)**

Product	AT25SL641-DWF																																																		
<b>Description</b>	64Mbit, Standard Serial Flash, 1.7V – 2.0V VCC																																																		
<b>Die Map</b>	 <p style="text-align: center;">Image reflects relative pad positioning only; not representative of actual die size.</p>																																																		
<b>Die Size &amp; Pad Coordinates</b>	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th></th> <th style="text-align: center;">X (μm)</th> <th style="text-align: center;">Y (μm)</th> </tr> </thead> <tbody> <tr> <td>Die Size<sup>(1)</sup></td> <td style="text-align: center;">3052</td> <td style="text-align: center;">1969</td> </tr> <tr> <td>Scribe Line Width</td> <td style="text-align: center;">60</td> <td style="text-align: center;">60</td> </tr> <tr> <td>Pad Opening</td> <td style="text-align: center;">65</td> <td style="text-align: center;">65</td> </tr> <tr> <td>CS</td> <td style="text-align: center;">-1232</td> <td style="text-align: center;">-558.5</td> </tr> <tr> <td>SO_IO1</td> <td style="text-align: center;">-1418</td> <td style="text-align: center;">-558.5</td> </tr> <tr> <td>WP_IO2</td> <td style="text-align: center;">-1418</td> <td style="text-align: center;">-688.5</td> </tr> <tr> <td>VCC</td> <td style="text-align: center;">1254</td> <td style="text-align: center;">-624.5</td> </tr> <tr> <td>VCC</td> <td style="text-align: center;">1174</td> <td style="text-align: center;">-624.5</td> </tr> <tr> <td>HOLD_IO3</td> <td style="text-align: center;">1418</td> <td style="text-align: center;">-624.5</td> </tr> <tr> <td>RESET</td> <td style="text-align: center;">1336</td> <td style="text-align: center;">-624.5</td> </tr> <tr> <td>SCK</td> <td style="text-align: center;">1406</td> <td style="text-align: center;">-818.5</td> </tr> <tr> <td>SI_IO0</td> <td style="text-align: center;">1406</td> <td style="text-align: center;">-900.5</td> </tr> <tr> <td>GND</td> <td style="text-align: center;">-1390</td> <td style="text-align: center;">-900.5</td> </tr> <tr> <td>GND</td> <td style="text-align: center;">-1304</td> <td style="text-align: center;">-900.5</td> </tr> <tr> <td>NC</td> <td style="text-align: center;">-1418</td> <td style="text-align: center;">-770.5</td> </tr> </tbody> </table> <p style="text-align: right; font-size: small;"><sup>(1)</sup> includes scribe line</p>				X (μm)	Y (μm)	Die Size <sup>(1)</sup>	3052	1969	Scribe Line Width	60	60	Pad Opening	65	65	CS	-1232	-558.5	SO_IO1	-1418	-558.5	WP_IO2	-1418	-688.5	VCC	1254	-624.5	VCC	1174	-624.5	HOLD_IO3	1418	-624.5	RESET	1336	-624.5	SCK	1406	-818.5	SI_IO0	1406	-900.5	GND	-1390	-900.5	GND	-1304	-900.5	NC	-1418	-770.5
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Technical Details	
Adesto Product Family	Standard Flash
Density	64 Mbit
Operating Vcc	1.7V - 2.0V
ESD	JESD22-A114
Delivery Option	Wafer- unsawn
Wafer Size (mm)	300 mm
Process Geometry (nm)	90 nm
Die ID	25M64
Wafer Map	Electronic- text file
Wafer Thickness (μm) Maximum	800
Back Grind Options	None / Contact Adesto
Back Plane Connection	Floating / Not Required
Backside preparation / metallization	None
Bond wire qualified	AU <input type="checkbox"/> CU <input type="checkbox"/> AG <input checked="" type="checkbox"/>
Passivation Material	PETEOS + SiON
Passivation Thickness (Å)	11000
Bond Pad Material	TaN/AlCu
Bond Pad Thickness (Å)	9500
Active Circuits underneath the bond pad	Yes

<sup>1</sup> Average value; subject to change without notice.

Part Number Ordering Code	Operating Temperature Range	Functional Specification
AT25SL641-DWF	-40°C to 85°C	<a href="http://www.adestotech.com/wp-content/uploads/AT25SL641_113.pdf">http://www.adestotech.com/wp-content/uploads/AT25SL641_113.pdf</a>

Revision Level – Release Date	History
A – August 2017	Initial release.

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