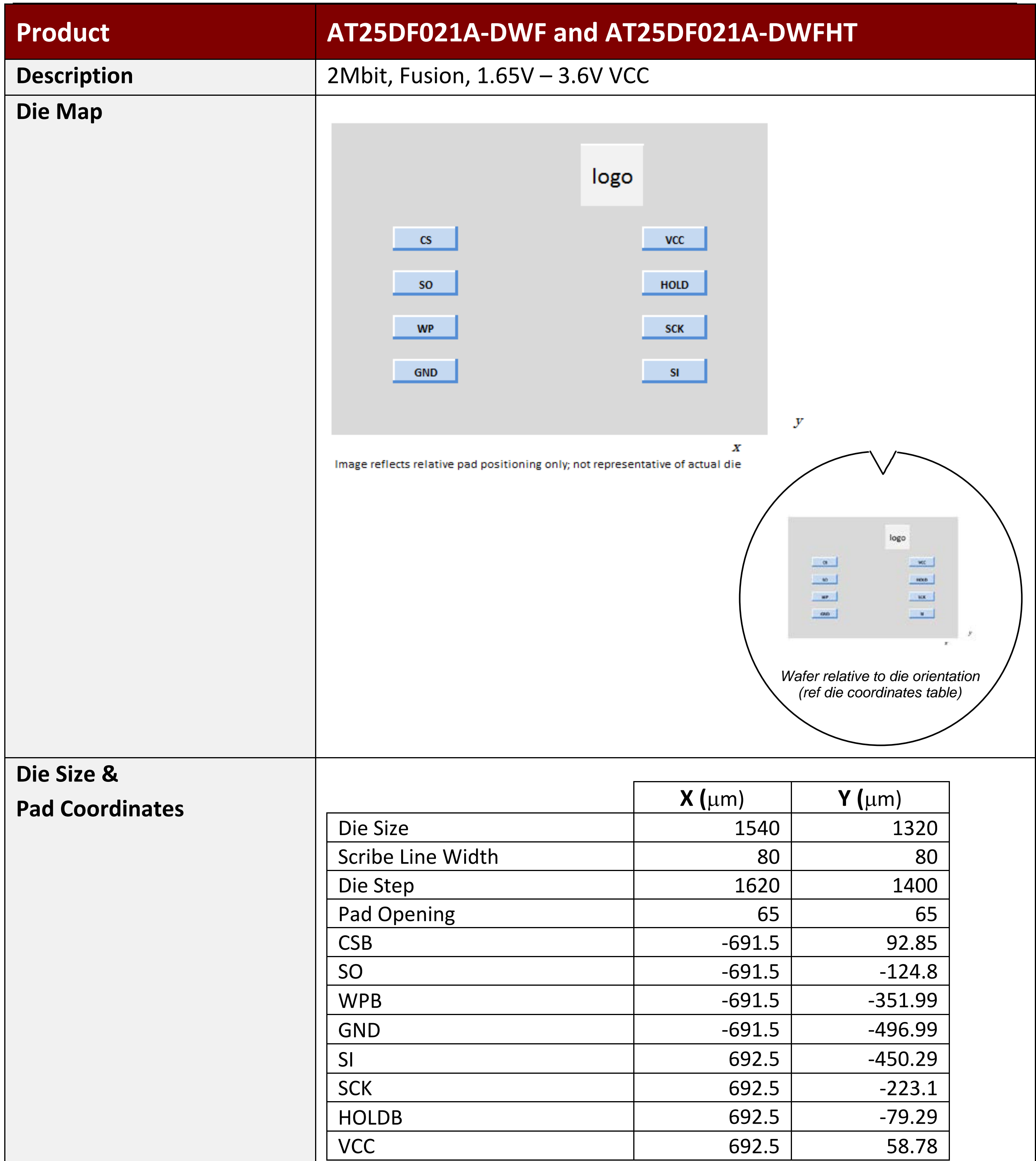
adesto® TECHNOLOGIES

AT25DF021A

2-Mbit, 1.65V Minimum
SPI Serial Flash Memory with Dual-I/O Support

WAFER PRODUCT DATASHEET (ADDENDUM)

Product	AT25DF021A-DWF and AT25DF021A-DWFHT
Description	2Mbit, Fusion, 1.65V – 3.6V VCC
Die Map	



Die Size & Pad Coordinates

	X (μm)	Y (μm)
Die Size	1540	1320
Scribe Line Width	80	80
Die Step	1620	1400
Pad Opening	65	65
CSB	-691.5	92.85
SO	-691.5	-124.8
WPB	-691.5	-351.99
GND	-691.5	-496.99
SI	692.5	-450.29
SCK	692.5	-223.1
HOLDB	692.5	-79.29
VCC	692.5	58.78

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Technical Details	
Adesto Product Family	Fusion
Density	2 Mbit
Operating Vcc	1.65V - 3.6V
ESD	>2kV JESD22-A114
Delivery Option	Wafer- unsawn
Wafer Size (mm)	200
Process Geometry (nm)	110
Die ID	637S4
Wafer Map	Electronic- text file
Manufacturing Facility	UMC
Wafer Thickness (µm) Maximum	725
Back Grind Options	None / Contact Adesto
Back Plane Connection	Floating / Not Required
Backside preparation / metallization	None
Bond wire qualified	AU ☒ CU ☐ AG ☐
Passivation Material	HDP oxide + SiON
Passivation Thickness (Å)	21000
Bond Pad Material	Ti/TiN/AlCu
Bond Pad Thickness (Å)	6000
Good Die per Wafer	Contact Adesto (AT25DF021A-DWF) [1]
Good Die per Wafer	Contact Adesto (AT25DF021A-DWFHT) [1]
Active Circuits underneath the bond pad	Yes

[1] Average value; subject to change without notice.

Part Number Ordering Code[2]	Operating Temperature Range	Functional Specification
AT25DF021A-DWF	-40°C to 85°C	http://www.adestotech.com/wp-content/uploads/DS-AT25DF021A-042.pdf
AT25DF021A-DWFHT	-40°C to 125°C	http://www.adestotech.com/wp-content/uploads/DS-AT25DF021A-HRADD.pdf

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[2] Handle product in accordance with UV and ESD precautions.

Revision Level – Release Date	History
A – August 2015	Initial release.
B – November 2015	Updated wafer orientation in die map image. Added footnote on handling.
C – August 2017	Updated address and contact information.

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