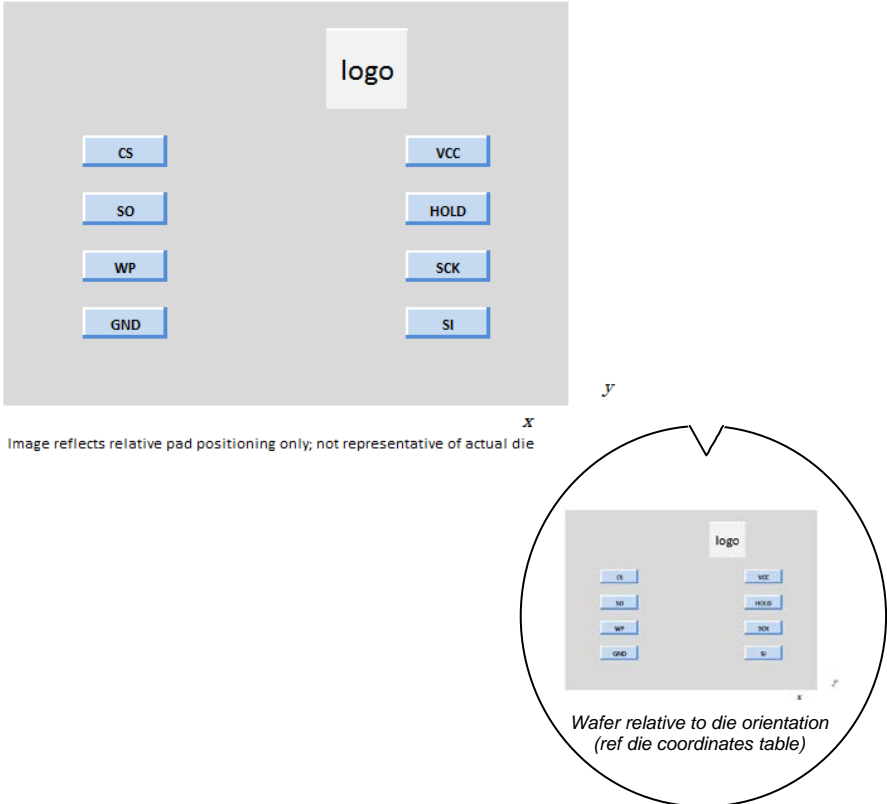


WAFER PRODUCT DATASHEET (ADDENDUM)

Product	AT25DF041B-DWF and AT25DF041B-DWFHT																																								
Description	4Mbit, Fusion, 1.65V – 3.6V VCC																																								
Die Map	 <p>Image reflects relative pad positioning only; not representative of actual die</p> <p>Wafer relative to die orientation (ref die coordinates table)</p>																																								
Die Size & Pad Coordinates	<table border="1"> <thead> <tr> <th></th> <th>X (μm)</th> <th>Y (μm)</th> </tr> </thead> <tbody> <tr> <td>Die Size</td> <td>1540</td> <td>1596</td> </tr> <tr> <td>Scribe Line Width</td> <td>80</td> <td>80</td> </tr> <tr> <td>Die Step</td> <td>1620</td> <td>1676</td> </tr> <tr> <td>Pad Opening</td> <td>65</td> <td>65</td> </tr> <tr> <td>CSB</td> <td>-691.5</td> <td>-45.15</td> </tr> <tr> <td>SO</td> <td>-691.5</td> <td>-262.8</td> </tr> <tr> <td>WPB</td> <td>-691.5</td> <td>-489.99</td> </tr> <tr> <td>GND</td> <td>-691.5</td> <td>-634.99</td> </tr> <tr> <td>SI</td> <td>692.5</td> <td>-588.29</td> </tr> <tr> <td>SCK</td> <td>692.5</td> <td>-361.1</td> </tr> <tr> <td>HOLDB</td> <td>692.5</td> <td>-217.29</td> </tr> <tr> <td>VCC</td> <td>692.5</td> <td>-79.22</td> </tr> </tbody> </table>			X (μm)	Y (μm)	Die Size	1540	1596	Scribe Line Width	80	80	Die Step	1620	1676	Pad Opening	65	65	CSB	-691.5	-45.15	SO	-691.5	-262.8	WPB	-691.5	-489.99	GND	-691.5	-634.99	SI	692.5	-588.29	SCK	692.5	-361.1	HOLDB	692.5	-217.29	VCC	692.5	-79.22
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Technical Details	
Adesto Product Family	Fusion
Density	4 Mbit
Operating Vcc	1.65V - 3.6V
ESD	>2kV JESD22-A114
Delivery Option	Wafer- unsawn
Wafer Size (mm)	200
Process Geometry (nm)	110
Die ID	637S5
Wafer Map	Electronic- text file
Manufacturing Facility	UMC
Wafer Thickness (µm) Maximum	725
Back Grind Options	None / Contact Adesto
Back Plane Connection	Floating / Not Required
Backside preparation / metallization	None
Bond wire qualified	AU <input checked="" type="checkbox"/> CU <input type="checkbox"/> AG <input type="checkbox"/>
Passivation Material	HDP oxide + SiON
Passivation Thickness (Å)	21000
Bond Pad Material	Ti/TiN/AlCu
Bond Pad Thickness (Å)	6000
Good Die per Wafer	Contact Adesto (AT25DF041B-DWF) ¹
Good Die per Wafer	Contact Adesto (AT25DF041B-DWFHT) ¹
Active Circuits underneath the bond pad	Yes

¹ Average value; subject to change without notice.

Part Number Ordering Code ²	Operating Temperature Range	Functional Specification
AT25DF041B-DWF	-40°C to 85°C	http://www.adestotech.com/wp-content/uploads/DS-AT25DF041B-040.pdf
AT25DF041B-DWFHT	-40°C to 125°C	http://www.adestotech.com/wp-content/uploads/DS-AT25DF041B-HRADD.pdf

Adesto Technologies Corporation

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² Handle product in accordance with UV and ESD precautions.

Revision Level – Release Date	History
A – August 2015	Initial release.
B – November 2015	Updated wafer orientation in die map image. Added footnote on handling.
C – August 2017	Updated address and contact information.

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