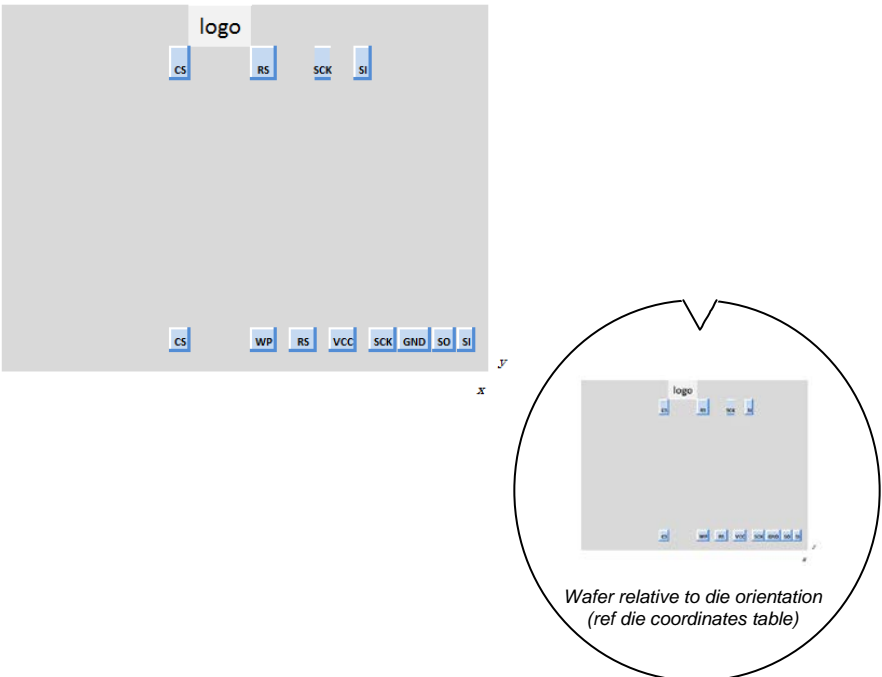


WAFER PRODUCT DATASHEET (ADDENDUM)

Product	AT45DB321E-DWF																																																				
Description	32 Mbit, DataFlash, 2.3V – 3.6V VCC																																																				
Die Map	 <p style="text-align: center;"><i>Wafer relative to die orientation (ref die coordinates table)</i></p>																																																				
Die Size & Pad Coordinates	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th></th> <th style="text-align: center;">X (μm)</th> <th style="text-align: center;">Y (μm)</th> </tr> </thead> <tbody> <tr> <td>Die Size</td> <td style="text-align: center;">3240</td> <td style="text-align: center;">3410</td> </tr> <tr> <td>Scribe Line Width</td> <td style="text-align: center;">80</td> <td style="text-align: center;">80</td> </tr> <tr> <td>Die Step</td> <td style="text-align: center;">3320</td> <td style="text-align: center;">3490</td> </tr> <tr> <td>Pad Opening</td> <td style="text-align: center;">65</td> <td style="text-align: center;">65</td> </tr> <tr> <td>SI</td> <td style="text-align: center;">1102.29</td> <td style="text-align: center;">1602.75</td> </tr> <tr> <td>SCK</td> <td style="text-align: center;">990.68</td> <td style="text-align: center;">1602.75</td> </tr> <tr> <td>RSB</td> <td style="text-align: center;">298.99</td> <td style="text-align: center;">1602.75</td> </tr> <tr> <td>CSB</td> <td style="text-align: center;">71.67</td> <td style="text-align: center;">1602.75</td> </tr> <tr> <td>WPB</td> <td style="text-align: center;">181.09</td> <td style="text-align: center;">-1602.85</td> </tr> <tr> <td>VCC</td> <td style="text-align: center;">479.27</td> <td style="text-align: center;">-1602.85</td> </tr> <tr> <td>GND</td> <td style="text-align: center;">1213.31</td> <td style="text-align: center;">-1602.35</td> </tr> <tr> <td>SO</td> <td style="text-align: center;">1342.99</td> <td style="text-align: center;">-1602.85</td> </tr> <tr> <td>SCK</td> <td style="text-align: center;">850.23</td> <td style="text-align: center;">-1602.35</td> </tr> <tr> <td>SI</td> <td style="text-align: center;">1477.35</td> <td style="text-align: center;">-1602.85</td> </tr> <tr> <td>CSB</td> <td style="text-align: center;">36.64</td> <td style="text-align: center;">-1602.35</td> </tr> <tr> <td>RSB</td> <td style="text-align: center;">361.51</td> <td style="text-align: center;">-1602.85</td> </tr> </tbody> </table>			X (μm)	Y (μm)	Die Size	3240	3410	Scribe Line Width	80	80	Die Step	3320	3490	Pad Opening	65	65	SI	1102.29	1602.75	SCK	990.68	1602.75	RSB	298.99	1602.75	CSB	71.67	1602.75	WPB	181.09	-1602.85	VCC	479.27	-1602.85	GND	1213.31	-1602.35	SO	1342.99	-1602.85	SCK	850.23	-1602.35	SI	1477.35	-1602.85	CSB	36.64	-1602.35	RSB	361.51	-1602.85
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Technical Details	
Adesto Product Family	DataFlash
Density	32 Mbit
Operating Vcc	2.3V - 3.6V
ESD	>2kV JESD22-A114
Delivery Option	Wafer- unsawn
Wafer Size (mm)	200
Process Geometry (nm)	110
Die ID	637F8
Wafer Map	Electronic- text file
Manufacturing Facility	UMC
Wafer Thickness (µm) Maximum	725
Back Grind Options	None / Contact Adesto
Back Plane Connection	Floating / Not Required
Backside preparation / metallization	None
Bond wire qualified	AU <input checked="" type="checkbox"/> CU <input type="checkbox"/> AG <input type="checkbox"/>
Passivation Material	HDP oxide + SiON
Passivation Thickness (Å)	21000
Bond Pad Material	Ti/TiN/AlCu
Bond Pad Thickness (Å)	6000
Good Die per Wafer	Contact Adesto ¹
Active Circuits underneath the bond pad	Yes

¹ Average value; subject to change without notice.

Part Number Ordering Code ²	Operating Temperature Range	Functional Specification
AT45DB321E-DWF	-40°C to 85°C	http://www.adestotech.com/wp-content/uploads/doc8784.pdf

² Handle product in accordance with UV and ESD precautions.

Adesto Technologies Corporation

3600 Peterson Way, Santa Clara, CA 95054 | phone: (408) 400-0578 fax: (408) 400-0721 | www.adestotech.com

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Revision Level – Release Date	History
A – August 2015	Initial release.
B – November 2015	Updated wafer orientation in die map image. Added footnote on handling.
C – August 2017	Updated address and contact information.

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